## REMARKS

<u>Summary of the Office Action</u>

Claims 1, 5, 57 and 59 are considered in the Office Action.

Claims 1, 5, 57 and 59 have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite because the claims include the trademark/trade name "VERILOG." In particular, the Final Action at 2 states that "the trademark VERILOG is used to describe a particular simulation environment."

Claims 1, 5, 57 and 59 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Joe LoCicero and Donald E. Thomas, "A Multithreaded Multiple-Language Hardware/Software Cosimulator," Carnegie Mellon University, Research Report No. CMUCAD-97-34, 1997 ("LoCicero")

<u>Reply to § 112, Second Paragraph Rejection</u>

The 22 November 2006 Final Office action (the "Final Action") states that claims 1, 5, 57 and 59 are indefinite because "the trademark VERILOG is used to describe a particular simulation environment." (Final Action at 2). Applicant respectfully disagrees that the previously presented claims included a trademark that was used as a limitation to identify or describe a particular material or product.

Nevertheless, to help move this case along, applicants have amended claims 1, 5, 57 and 59. In particular, the claims recite a "simulator that runs VERILOG code." Because the amended claims do not recite a "particular simulation environment," as interpreted in the Final Action, applicants respectfully request that the Examiner withdraw the § 112, second paragraph rejections.

<u>Reply to § 102(b) Rejection</u>

Applicants have amended claim 1, 5, 57 and 59 to more particularly point out and distinctly claim the invention. In particular, amended claims 1 and 59 recite methods for providing a design test bench, the methods including, among other things, providing a single executable program adapted to create a primary thread and one or more secondary threads, the primary thread running VERILOG code on a simulator that runs VERILOG code, each of the secondary threads running a corresponding interpreter

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that interprets an associated scripted routine, each scripted routine comprising an associated user-defined call that is mapped to a VERILOG task.

"[F]or anticipation under 35 U.S.C. 102, the reference must teach every aspect of the claimed invention either explicitly or implicitly." MPEP 706.02 (emphasis added). LoCicero does not teach every aspect of the claimed invention either explicitly or implicitly. In particular, unlike the claimed invention, LoCicero does not describe or suggest methods that provide a single executable program adapted to create a primary thread running VERILOG code on a simulator that runs VERILOG code, and a secondary thread running an interpreter that interprets a scripted routine comprising a user-defined call that is mapped to a VERILOG task.

Indeed, LoCicero does not describe anything regarding a single executable program that creates such primary and secondary threads, and the Final Action does not identify any such specific teaching. Instead, the Final Action states that LoCicero "describ[es] a cosimulation environment for Verilog and C++ code." Final Action at 5 (citing LoCicero pp 6-11 and 16-18). Such a broad and generalized statement fails to show that the reference teaches every aspect of the claimed invention.

Unlike the claimed invention, LoCicero does not describe anything about a single executable program that creates a primary thread and a secondary thread, wherein the primary thread runs VERILOG code on a simulator that runs VERILOG code. Indeed, LoCicero does not describe anything about such a single executable program that creates such first and second threads. Instead, LoCicero describes a "cosimulator" environment in which VERILOG code is converted to "an internal, stylized form of C++," and then the converted code is compiled and linked with C++ functions to form a completed simulation environment. (Page 6; FIG. 1).

Thus, LoCicero not only fails to describe the claimed single executable program, LoCicero also fails to describe a single executable program that creates a primary thread that runs VERILOG code on a simulator that runs VERILOG code. The Final Action states that "the internal conversion of VERILOG code does not change the fact that the LoCicero system simulates VERILOG code. . . . VERILOG code goes in, and simulation results come out. . . . It is clear from the disclosure of LoCicero . . . [that] the simulation engine of LoCicero may be considered a VERILOG simulator." (Final Action at 3-4).

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Even if this were correct, the claims do not merely recite a system that "simulates VERILOG code," or that "may be considered a VERILOG simulator." In this regard, the Final Action seems to suggest that a prima facie case of anticipation in this case may somehow be established by citing any reference that describes any system that "simulates VERILOG code," or that "may be considered a VERILOG simulator."

LoCicero does not explicitly or implicitly describe the <u>claimed</u> invention, which requires providing a <u>single executable program</u> adapted to create a primary thread running VERILOG code on a simulator that runs VERILOG code, and a secondary thread running an interpreter that interprets a scripted routine comprising a user-defined call that is mapped to a VERILOG task. Instead, LoCicero expressly points away from the claimed invention by describing a system that implements a simulator that runs C++ code, not VERILOG code.

Because LoCicero does not describe the claimed invention, and actually points away from the claimed invention, applicants respectfully request that the § 102(b) rejections of claims 1 and 59 be withdrawn. Because claims 5 and 57 depend from claim 1, applicants further respectfully request that the § 102(b) rejections of claims 5 and 57 be withdrawn

Conclusion

For the reasons stated above, applicants submit that this application, including claims 1, 5, 57 and 59, is allowable. Applicants therefore respectfully request that the Examiner allow this application.

Respectfully submitted,

James Trosino
Registration No. 39,862
Attorney for Applicants

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